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SUBSTITUTE SPECIFICATION

EQUALIZER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention refers to a method to equalize signals transmitted on a line as well as an equalizer filter realized in CMOS technology and besides an integrated circuit comprising an equalizer circuit.

Description of the Related Art

In high speed line communications, for instance in the case of data transmission of SDH equipment, the only filtration of the received signal is not sufficient to recover the data with a small error rate. An equalizer circuit is therefore necessary to compensate the line loss and improve the intersymbol interferences of the datum to recover. As known the line dispersion losses are linearly proportional to the length of the line and besides they are proportional to the square root of the frequency of transmission. The equalizer must therefore have a frequency response inversely proportional to that of the line. Particularly it is necessary an adaptive equalizer able to deal with variable lengths of line without altering significantly the intersymbol interferences.

BRIEF SUMMARY OF THE INVENTION

An embodiment of the present invention realizes an equalizer able to compensate the line attenuations in a simple and effective way.

Another embodiment of the invention is directed to a method that equalizes signals transmitted on a line comprising the following phases: applying an analog adaptive filter in series with said line, having a working frequency band and having at least one pole and at least one zero the position of which in said working frequency band is variable in response to the attenuation of said line; applying a retroaction circuit to the output of said filter able to vary the position of said at least one pole and at least one zero; setting said at least one pole and at least

one zero in correspondence to a prefixed frequency of said working frequency band; moving the position of said at least one pole toward the high frequencies at the increasing of said attenuation of said line; and moving the position of said at least one zero toward the low frequencies at the increasing of said attenuation of said line.

An equalizer circuit according to an embodiment of the present invention equalizes signals transmitted on a line having an attenuation comprising: an analog adaptive filter applied in series to said line comprising plural transconductance filters having a bias current each and to which it is associated at least one pole and at least one zero the position in frequency of which in the working band is variable in response to said bias current; a retroaction circuit applied to the output of said filter able to vary said bias current; said bias current varies at the varying of said attenuation of said line; wherein said transconductance filters have said bias current of prefixed value; said bias current is made to vary at the increasing of said attenuation so that said at least one pole is moved toward the high frequencies; and said bias current is made to vary at the increasing of said attenuation so that said at least a zero is moved toward the low frequencies. The equalizer circuit can be an integrated circuit of CMOS type

Thanks to the present invention it is possible to realize a linear equalizer that does not require of any external regulation. It results to be very simple as the retroaction loop checks only the output voltage. Besides realizing it completely in CMOS technology it is possible to integrate it with other circuits on a single chip.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The characteristics and the advantages of the present invention will result evident from the following detailed description of one of its embodiment, illustrated as example not limitative in the joined sketches, in which:

Figure 1 shows a blocks scheme of an equalizer according to the present invention;

Figure 2A shows a schematic circuit of an example of a transconductance filter and the Figure 2B its Bode diagram;

Figure 3 shows a schematic circuit of an example of a circuit 4 that provides an indication of the variation of the line attenuation;

Figure 4 shows a schematic circuit of an example of the circuit of charge pump 5;

Figure 5 shows a schematic circuit of an example of a variable bias generator 7;

Figure 6 shows a diagram that shows the course of the voltage to the terminal of the capacitor 6 and the course of the control current of the adaptive filter 1;

Figure 7 shows a diagram that shows the positioning and the variations of the poles/zeros in the frequency plane;

Figure 8 shows a diagram that shows the course of the transfer function of the filter 1 in the frequency at the varying of the line attenuation; and

Figure 9 shows a schematic circuit of a bias generator 8 dependent on the process.

DETAILED DESCRIPTION OF THE INVENTION

A block scheme of an equalizer according to an embodiment of the present invention, shown in Figure 1, comprises an input signal 10, coming from a line, applied to an adaptive filter 1 which provides an output 11. The signal at the output of the adaptive filter 1 is applied to a comparator 3 that compares this signal 11 with a reference voltage 13. At the output of the comparator 3 there is a filter 14 composed of a first circuit 4 that provides an indication of the variation of the line attenuation, connected to a charge pump 5 which in turn is connected to a capacitor 6. The circuit 4 is sampled by a working frequency 15. The voltage at the terminals of the capacitor 6 is applied to a variable bias generator 7. To the generator 7 are applied, preferably, also the signals Pr1-Prm coming from a bias generator 8 dependent on the process. The signals Pc1-Pcn in output from the generator 7 are applied to the adaptive filter 1.

The filter 1 comprises preferably adaptive filters of the transconductance type with biquadratic cells, for instance in Figure 2A is drawn the block scheme of a transconductance filter having one pole which has an input 20 and it comprises a first stage 21 having transconductance Gm, and a second stage 22 having transconductance GmD, an output 23. Between the first stage 21 and the second stage is connected a capacitor C. To the first stage 21 is connected a terminal Pc1 and to the second stage 22 is connected a terminal Pc2, which

receives the bias current. The bias current Pc2 varies the GmD transconductance of the circuit which varies the position of the pole in frequency in the working band accordingly. In fact it could be seen from the Figure 2B, where it is represented the Bode diagram of the circuit of Figure 2A, that the position of the pole in frequency is given by the division GmD/C and the point in which the gain module is equal to 1 it is equal to Gm/C. Therefore, varying the bias current Pc2, varies the value of GmD and therefore the pole frequency position. The bias current Pc1 varies the Gm transconductance of the circuit which, if varied in a separate way as regards the current Pc2, varies the continuous gain accordingly, which as shown in Figure 2B is equal to Gm/GmD. If the bias currents Pc1 and Pc2 vary equally, then the pole position moves but the continuous gain does not vary.

To each filter of this type could be associated either one pole or one zero in accordance to the particular type of circuit. To be able to vary the position of each pole and of each zero it is necessary a bias current for each of them and a current to make vary (increase) the continuous gain of a prefixed value. In an example of realization of the present invention, the filter 1 comprises two biquadratic filters and one at a single stage, for a total of 5 poles and of 5 zeros. Such types of filters are well known by the skilled in the art, and they are not furtherly described, an example of such filters could be found in the article of F. Rezzi, I. Bietti, M. Cazzaniga and R. Castello by the title "A 70 mW seventh order filter with 7-50 MHz cut-off frequency and programmable boost and group delay equalization" published in the IEEE Journal of solid state circuits, vol. 32, No. 12, December 1997.

The signals Pc1-Pcn correspond to the bias current (variable at the varying of the line attenuation) of the transconductance filters; preferably these bias currents are compensated by the Pr1-Prm signals that correspond to the currents supplied by the bias generator 8 which depend on the thermal and constructive variations of the device.

A schematic circuit of an example of the line attenuator detector 4 that supplies an indication of the variation of the line attenuation, shown in Figure 3, comprises a first bistable circuit 31 of D type and a second bistable circuit 32 of D type. The output of the comparator 3 is applied to a terminal 35 of the first bistable circuit 31 which corresponds to the reset input R of the circuit and also to an input of a NOR circuit 33, the output Q of which is connected to the

input D of the bistable 31. The output Q of the bistable 31 is applied the input D of the second bistable circuit 32, the output Q of which is applied to the output terminal 36. The output Q of the bistable 31 is also applied to the second input of the NOR circuit 33. A clock signal is applied to the terminal 15 that it is connected to the clock input of the bistable 32 and it is also connected to the clock input of the bistable 31 through an inverter circuit 34.

A schematic circuit of an example of the charge pump circuit 5, shown in Figure 4, comprises a first transistor 41 with p-channel and a second transistor 42 with n-channel having the gates connected together in order to form an input terminal 36 (connected to the output of the circuit 4), the source of the transistor 41 is connected to the supply voltage, the transistor source 42 is connected to ground, the drain of the transistor 42 is connected to the drain of the transistor 41 and they are connected to a terminal 44 of the capacitor 6, the other terminal of the capacitor 6 is set to ground. If the input signal 36 of the charge pump circuit 5 is at high level, the capacitor 6 discharges itself, if the signal is at a low level the capacitor 6 charges itself.

The whole of the circuits 4, 5 and 6 constitute the filter 14 that integrates the signal in output from the comparator 3 and it provides in output a signal proportional to the course of the line attenuation that is used to predispose the bias and control current Pc1-Pcn of the filter 1.

Particularly, the circuit 4 drawn in Figure 3 provides in output a signal, for instance of high level, if the signal output from the comparator 3 remains high for at least one clock cycle of the working frequency 15. By varying the working frequency 15, it is possible to vary the reaction times of the circuit in response to the line attenuation varying. The charge pump 5 charges and discharges the capacitor 6 so that the voltage across the capacitor is proportional to the value of line attenuation opportunely filtered.

A schematic circuit of an example of a variable bias generator 7, shown in Figure 5, comprises an n-channel transistor 45 having a gate connected to a terminal 44 to which has been applied the voltage present on the capacitor 6, a source connected to ground, and a drain connected to a branch of a first current mirror 46 which is connected to the supply voltage Vcc through a p-channel transistor 47. The other branch of the current mirror 46 is connected to a branch of a second current mirror 48, and in the other branch of the second current mirror 48

flows a current Ic1 and corresponds to the terminal Pc1. The drain of the transistor 45 is connected also to the source of an n-channel transistor 49. The drain of the transistor 49 is connected to a branch of a third current mirror 50 which is connected directly to the supply voltage Vcc. The other branch of the third current mirror 50 is connected to a branch of a fourth current mirror 51, and in the other branch of the fourth current mirror 51 flows a current Ic2 and corresponds to the terminal Pc2. The gate of the transistor 49 is connected to the drain of a transistor 53 having a source connected to ground and a gate connected to the terminal Pr1. The gate of the transistor 49 is also connected to a p-channel transistor 52 connected like a diode, to which is applied the supply voltage Vcc and which forms a current mirror together with the transistor 47, the two gates of the two transistors 47, 52 being connected together.

In Figure 5, only for representation simplicity have been drawn only the circuits that provide current to the two terminals Pc1 and Pc2 of the filter 1 depending on the value of the input Vc of the capacitor 6 and of the input Pr1 coming from the bias generator 8. Also in this case it has been considered for representation simplicity only one terminal of the plurality of the terminals Pr1-Prm.

The variable bias generator 7 must provide the bias currents by the terminals Pc1-Pcn to the various transconductance filters present in the filter 1. Such bias currents must be placed at quiescent (Vc= 0), for instance placed for a line having length equal to 0 and they therefore must vary at the varying of the line attenuation. The generator 7 receives in input the Vc signal from the capacitor 6 and is able to absorb the current Ic1 (from the terminal Pc1). The current Ic1, which starting from Vc equal to null, linearly increases at the increasing of Vc, up to a limit of current equal to Ip/2, where Ip is the flowing current in the transistor 53, after that it begins to increase linearly the current Ic2, (up to a possible circuital limit). The current Ip could be generated by a fixed generator Ip but, the equalizer circuit comprises besides preferably the bias generator 8 which provides a bias current able to compensate the thermal and constructive variations of the equalizer. For instance at the increasing of the temperature the current Ip increases according to the variation of the bias present on the terminal Pr1.

In Figure 6 could be seen the waveforms of some signals of the circuit of Figure 5. Particularly it is possible to see the exponential relationship between the input voltage Vc

applied to the terminal 44 of the transistor 45 and its relative drain current Ic. Moreover it is possible to see the course of the current Ic1 and Ic2 flowing respectively in the mirrors 48 and 51 and correspondent to the bias and control current present on the terminals Pc1 and Pc2.

As already said, Figure 5 represents for simplicity a reduced circuit able to provide only two currents to the terminals Pc1 and Pc2. However, one can imagine a series of currents one for each pole and one for each zero present in the filter 1 and also the current or preferably the currents necessary to increase the continuous gain. The currents relative to each couple of poles/ zeros, positioned in frequency in the same place, will have a similar course as, better explained further on, they will have to move simultaneously, after that the couple of poles/zeros placed immediately at a smaller frequency will move.

Figure 7 shows a diagram that shows the positioning of the poles/zeros in the frequency plane, particularly it is possible to note the uniform spacing between the couples of poles/zeros along a logarithmic frequency axis inside the band B of the working frequencies of the filter. Besides it is possible to note the displacement direction that the poles and the zeros effect at the varying (at the increasing) of the line attenuation, in response of the variations of the bias current to the terminals Pc1-Pcn. Particularly the poles move toward the high frequency and the zeros move toward the low frequency. Besides the couples of poles/zeros move in succession (in the indicated direction) beginning from the identifying number 71 up to the number 75, finally the filter continuous gain increases and makes the opportune bias currents vary. In practice, the pole and the zero of the couple 71 placed at high frequency inside the working band move first, then in succession the pole and the zero of the couple 72 move next and so forth up to the movement of the couple 75 placed at a lower frequency. Therefore, when all the couples have moved, the continuous gain is increased. All the displacement above reported are effected in consequence of the variations of the bias and control current present on the terminals Pc1-Pcn.

In one embodiment, the pole and zero are moved approximately 30% compared to their initial position.

In Figure 8 is shown a diagram of the transfer function of the filter 1 in function of the frequency at the varying of the line attenuation, the arrow points out as varies the transfer function at the increasing of the line attenuation. At the moving of the couples of poles/zeros

above mentioned it is possible to see in Figure 8 the variation of the transfer function and particularly it is possible to see that only at the end the continuous gain is varied.

A schematic circuit of an example of a bias generator 8 dependent from the process, shown in Figure 9, comprises a plurality of n-channel transistors 61 and 62 having sources connected to ground, drains respectively connected to the terminals Pr1-Prm, and gates connected together and connected to a node connected to a gate of a transistor 63, a terminal of a generator of current Iref 67, and a branch of a first current mirror 68. The source of the transistor 63 is connected to ground and the drain is connected to the source of a differential couple formed by the n-channel transistors 64 and 65 having gates respectively connected to two reference voltages Vref1 and Vref2, with Vref2>Vref1, and drains connected to a second current mirror 66 connected to the power supply Vcc. The drain of the transistor 64 is also connected to a branch of the mirror 68. This circuit generates currents able to compensate the variations in temperature, of the supply voltage and of the dispersions of the characteristics (from device to device) due to the construction process.

In accordance to the present invention it is possible to realize a device in CMOS technology at low cost with the possibility of being integrated with other circuits on the same chip where external circuits are not required. Besides a good equalization with a reduced number of poles and zeros is obtained, in fact with 5 poles and 5 zeros and an equalization band of 260 MHz it is possible to equalize signals transmitted on a line of length of about 350 m.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

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